



Description

JMT N-channel Enhancement Mode Power MOSFET

Features

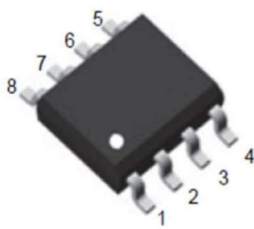
- 40V, 10A
 $R_{DS(ON)} < 14.3m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 19.6m\Omega @ V_{GS} = 4.5V$
- Lead free and Green Device Available
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

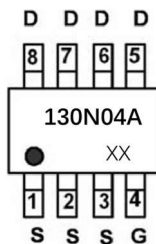
- Load Switch
- PWM Application
- Power management



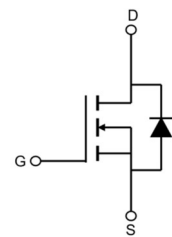
100% UIS TESTED!
100% ΔVds TESTED!



SOP-8 top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
130N04A	JMTP130N04A	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	40	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	10
		$T_A = 100^\circ\text{C}$	6.5
I_{DM}	Pulsed Drain Current ^{note1}	40	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	6.8	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	2.5
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	$^\circ\text{C/W}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.5	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note3</small>	V _{GS} =10V, I _D =10A	-	11	14.3	mΩ
		V _{GS} =4.5V, I _D =5A	-	14	19.6	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1.0MHz	-	1250	-	pF
C _{oss}	Output Capacitance		-	114	-	pF
C _{rss}	Reverse Transfer Capacitance		-	85	-	pF
Q _g	Total Gate Charge	V _{DS} =20V, I _D =5A, V _{GS} =10V	-	20	-	nC
Q _{gs}	Gate-Source Charge		-	3.5	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	4.2	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =10A, R _L =1Ω, R _{GEN} =3Ω, V _{GS} =10V	-	10	-	ns
t _r	Turn-on Rise Time		-	9	-	ns
t _{d(off)}	Turn-off Delay Time		-	32	-	ns
t _f	Turn-off Fall Time		-	16	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	10	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	40	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =10A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	T _J =25°C, I _F =10A, di/dt=100A/μs	-	22	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	11	-	nC

- Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
 2. EAS condition: T_J=25°C, V_{DD}=20V, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=5.2A
 3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

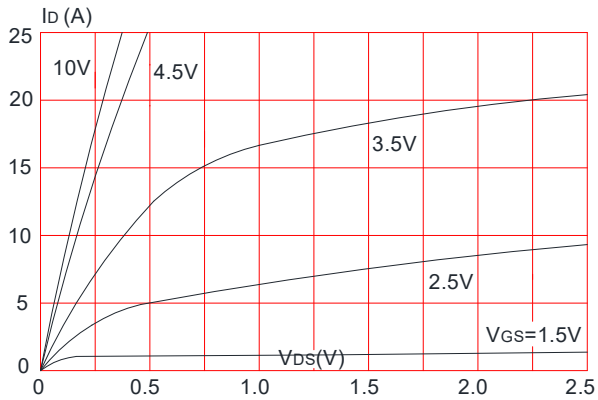


Figure 2: Typical Transfer Characteristics

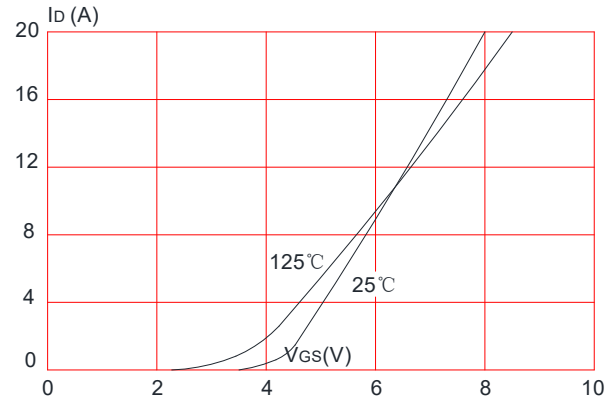


Figure 3: On-resistance vs. Drain Current

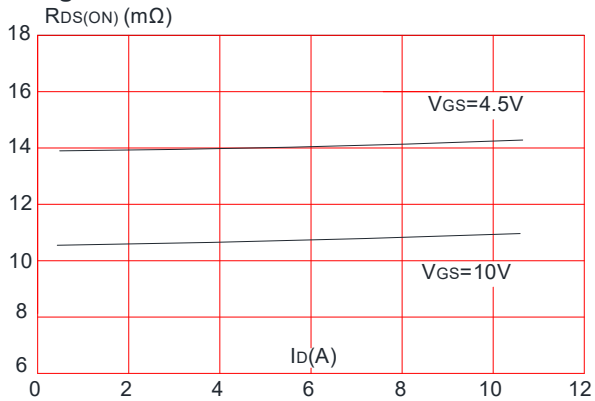


Figure 4: Body Diode Characteristics

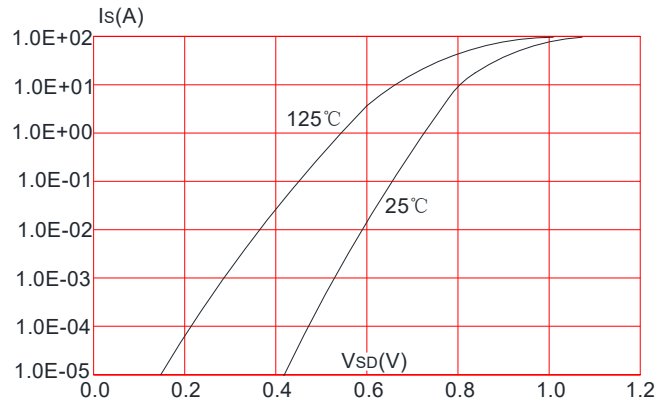


Figure 5: Gate Charge Characteristics

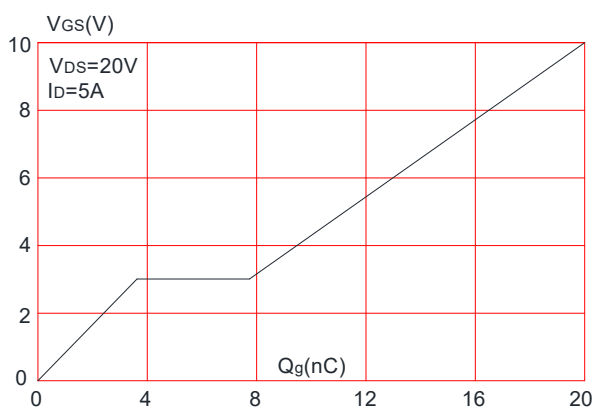


Figure 6: Capacitance Characteristics

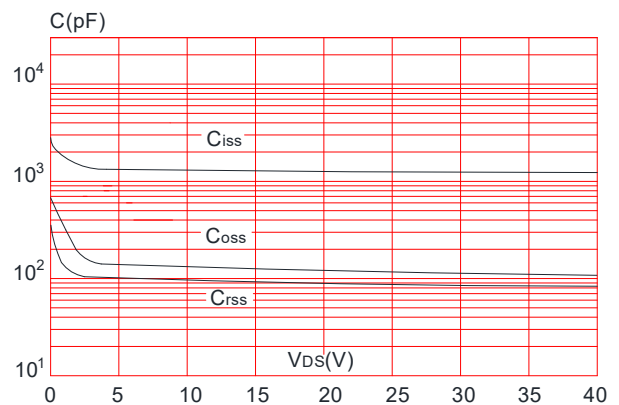




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

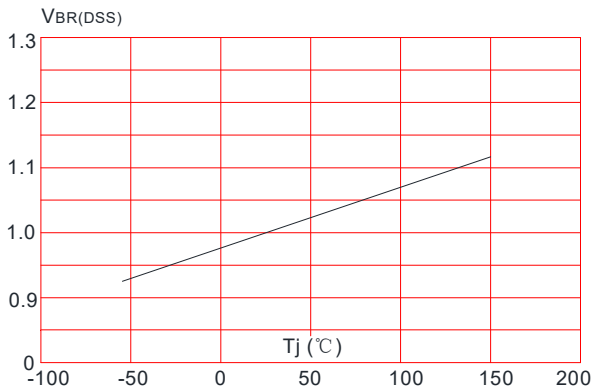


Figure 8: Normalized on Resistance vs. Junction Temperature

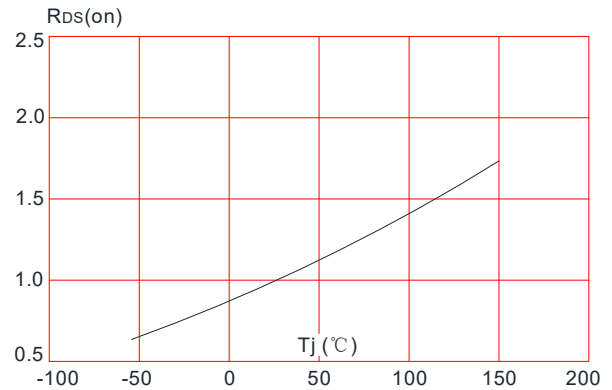


Figure 9: Maximum Safe Operating Area

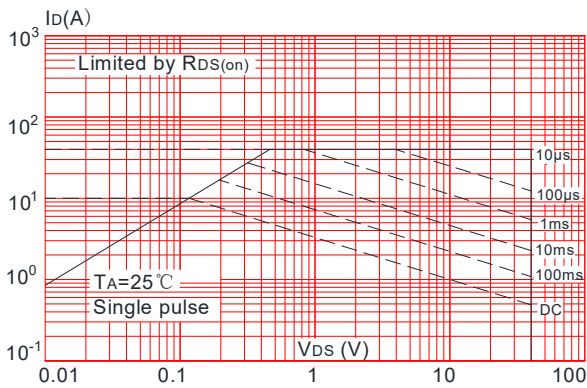


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

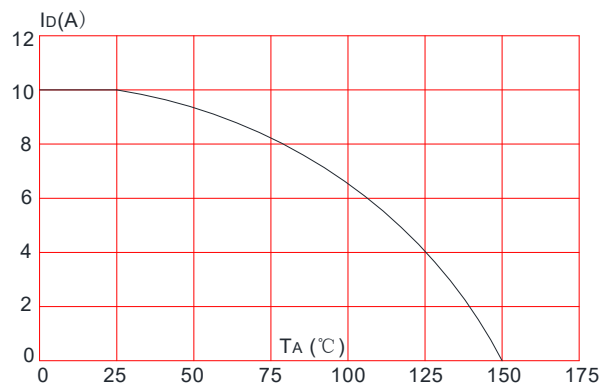
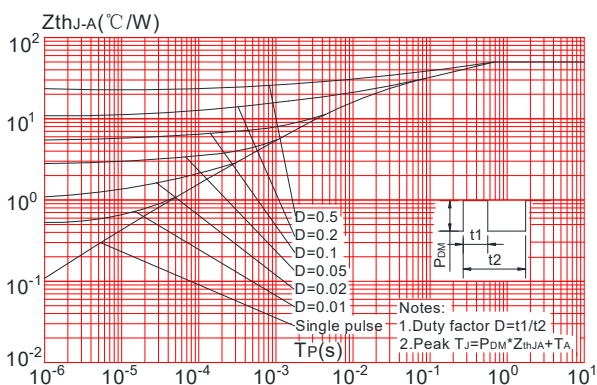


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit



Figure 1: Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

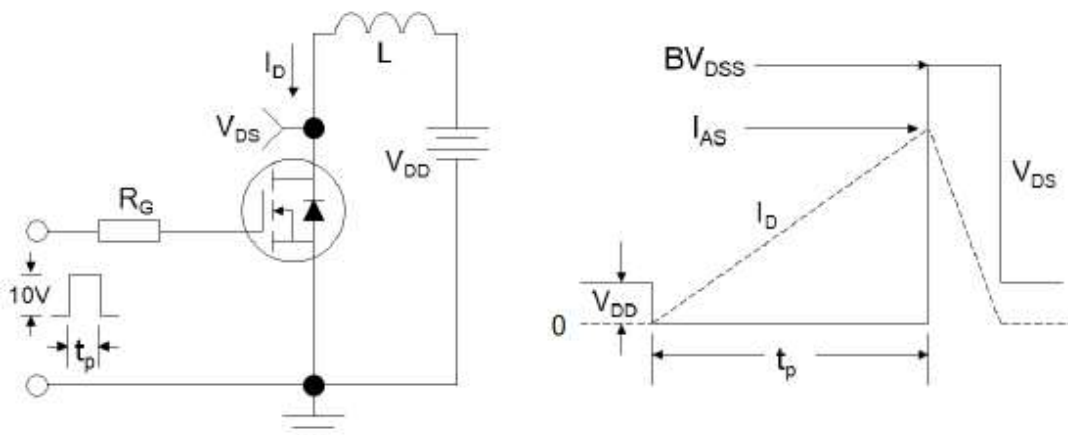
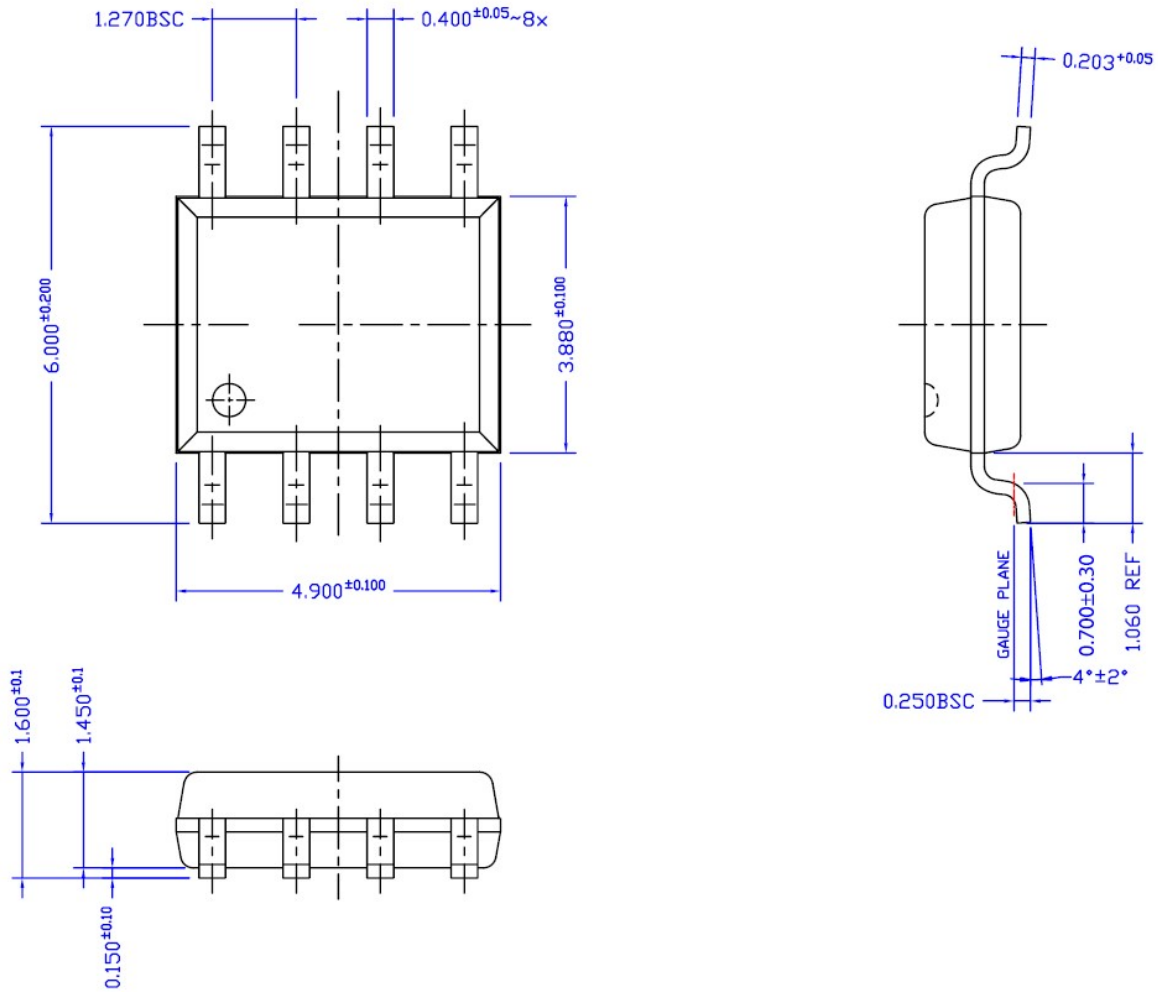


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-SOP-8



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